Vacancy Name: **IC Verification Manager**

Location City: Thalwil

Location Country: Switzerland

Role also available in: Athens, Greece-Leuven, Belgium- Malmo, Sweden

**About u-blox**

Swiss-based u-blox (SIX: UBXN) is the global leader in wireless and positioning semiconductors for the automotive, industrial and consumer markets. Our solutions enable people, vehicles and machines to locate their exact position and wirelessly communicate via voice, text or video. With a broad portfolio of chips, modules and software solutions, u-blox is uniquely positioned to allow OEMs to develop innovative solutions that enable mobility quickly and cost-effectively. With headquarters in Thalwil, Switzerland, u-blox is globally present with offices in Europe, Asia and the USA.

**Job Description**

The IC Verification Manager is responsible for defining optimal verification method and its proper execution. He is in charge for both human and infrastructure resource management as well as for tasks definition and allocation. The IC Verification Manager writes and runs test cases and test benches.

**Tasks**

* Manage resources and tasks in the verification team
* Define best verification methodology for different projects
* Collect and manage functional requirements
* Define verification requirements and test plan for all the projects
* Write test cases and drivers in C for top-level verification
* Write test benches in System Verilog in a UVM environment
* Ensure performance to specification and readiness for production
* Investigate and introduce accelerators for hardware/software co-verification and system-level verification
* Technical reporting both written and oral
* Support design team in block level verification and in silicon characterization
* Digital design
* Responsible for defining best verification/validation methodology
* Responsible for meeting optimal verification coverage in projects
* Responsible for investigating new opportunities in verification/validation methods
* Responsible to meet quality standards in design flow
* Responsible for IP and top-level verification
* Responsible verification methodology alignment and deployment in different sites/projects

**Requirements**

* Master Degree in Electrical Engineering
* 10+ years experience in verification: UVM, C-code test case, System Verilog, formal verification, System Verilog/VHDL test bench, Palladium Emulation, FPGA prototyping
* Proven track record in leading teams
* Excellent skills in ASIC verification tool usage, e.g. Synopsys, Modelsim, Cadence
* Experience in verifying multiple power and clock domains designs
* Experience with Palladium Accelerator wished
* Used to work independently and precisely
* Good communications skills Fluent in English and German
* Swiss- or EU-citizen or valid work permit for Switzerland

**Contact**

Are you interested in this challenging position within an international work environment in a successful company? Apply now! You will be working with a motivated team in an exciting technology.

We are looking forward to receiving your application.

https://ublox.secure.force.com/recruit/fRecruit\_\_ApplyJob?vacancyNo=VN708